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EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,765	HERNER, S. BRAD	
	Examiner	Art Unit	
	Jay C. Kim	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/28/07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-16, 18-20, 27, 28, 30-57* is/are pending in the application.

4a) Of the above claim(s) *45-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-16, 18-20, 27, 28, 30-44 and 57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/3/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Request for Continued Examination filed March 28, 2007.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 57, 2, 3, 6, 8, 15, 35, 36 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295).

In regards to claim 57, Cutter et al. disclose a semiconductor device (Fig. 6B) comprising a silicide layer (642) (col. 8, line 1), a dielectric antifuse layer (610) (col. 8, lines 15-21) on and in contact with the silicide layer (642), and a conductive layer or semiconductor layer (614) (col. 8, lines 24 and 27-28) on and in contact with the dielectric antifuse layer (610), wherein the silicide layer (642) and the dielectric antifuse layer (610) are portions of the semiconductor device (Fig. 6B).

It is inherent that the dielectric antifuse layer has suffered dielectric breakdown such that an electrical connection exists between the silicide layer and the conductive layer or semiconductor layer in the antifuse semiconductor device.

Cutter et al. differ from the claimed invention by not showing that the dielectric antifuse layer is a grown dielectric antifuse layer.

Mayer et al. disclose oxidation of silicides (**10.7** Oxidation of Silicides and Fig. 10.19) to grow dielectric SiO_2 on a silicide (lines 5-7 of **10.7** Oxidation of Silicides).

Since both Cutter et al. and Mayer et al. teach a method of fabricating a semiconductor device comprising a silicide layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. with the grown dielectric SiO_2 layer on a silicide layer disclosed by Mayer et al. to form an antifuse semiconductor device where a grown SiO_2 dielectric layer is on and in contact with the silicide layer while the rest of the dielectric antifuse layer can be formed by deposition, because the combined semiconductor device would have a grown dielectric SiO_2 layer with less contamination and thus of better quality due to the fact that the SiO_2 layer can be grown right after silicide formation.

In regards to claim 2, Cutter et al. further disclose that the silicide (642) is a refractory metal silicide (col. 8, line 1), which can be niobium silicide or tantalum silicide.

In regards to claim 3, Cutter et al. further disclose that the antifuse layer (610) may comprise silicon dioxide (col. 8, lines 17-19).

In regards to claim 6, Cutter et al. further disclose for the semiconductor device of claim 2 that the conductive layer or semiconductor layer (614) on and in contact with the antifuse layer (610) may be a metal layer (col. 8, lines 27-28).

In regards to claim 8, Cutter et al. further comprise a first silicon layer (640) (col. 8, line 2), the silicide layer (642) on and in contact with the first silicon layer (640).

In regards to claim 15, Cutter et al. further disclose for the semiconductor device of claim 6 that the conductive layer (614) comprises a metal (col. 8, lines 27-28).

In regards to claim 35, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer was grown by oxidizing or nitriding the silicide.

Mayer et al. disclose oxidation of silicides (**10.7** Oxidation of Silicides and Fig. 10.19) to grow dielectric SiO_2 on a silicide layer (lines 5-7 of **10.7** Oxidation of Silicides).

Since both Cutter et al. and Mayer et al. teach a method of fabricating a semiconductor device comprising a silicide layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the dielectric SiO_2 layer grown by oxidizing the silicide disclosed by Mayer et al., because the combined semiconductor device would have a dielectric SiO_2 layer with less contamination and thus of better quality due to the fact that the SiO_2 can be grown right after silicide formation.

In regards to claim 36, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.

Cutter et al. further disclose that the silicide layer (642) is in contact with the polysilicon layer (640) (col. 8, line 2 and Fig. 6B).

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the polysilicon layer in contact with the silicide layer is lightly doped or intrinsic, and therefore the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between a Schottky diode and a conductor.

Cutter et al. further disclose that the bottom conductor (112) (col. 1, line 21) of a semiconductor device (Fig. 1) comprising an antifuse layer (110) (col. 1, line 20) is in contact with n- region (126), forming a Schottky diode.

Since Cutter et al. teach a method of fabricating a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the Schottky diode structure disclosed by Cutter et al. to make a semiconductor device comprising a Schottky diode formed between the silicide layer as a bottom conductor and the semiconductor n-region at the bottom and a conductor at the top, because the combined semiconductor device would form a diode device after programming the antifuse layer.

In regards to claim 40, Cutter et al. further disclose that the silicide (642) is a portion of the Schottky diode (640 and 642 combined).

3. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 2 above, and further in view of Arghavani et al. (US 5,780,346). The teachings of Cutter et al. in view of Mayer et al. are discussed above.

In regards to claim 4, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.

Cutter et al. further disclose that the dielectric antifuse layer (610) may comprise a combination of layers (col. 8, lines 21-22), which can be silicon dioxide and silicon nitride (col. 8, lines 17-19).

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer comprises nitrogen.

Arghavani et al. disclose a semiconductor device (Fig. 3K) where silicon oxynitride (365 and 366) (col. 6, lines 15 and 16) is formed by nitridation of silicon oxide (360) (col. 5, lines 66 - col. 6, line 2).

Since both Cutter et al. and Arghavani et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the oxynitride layer disclosed by Arghavani et al. to have the grown dielectric antifuse layer comprise nitrogen, because the combined semiconductor device would prevent dopant outdiffusion from the silicide layer or polysilicon layer when polysilicon is used as a semiconductor layer on and in contact with the antifuse layer.

In regards to claim 5, Cutter et al. in view of Mayer et al. and further in view of Arghavani et al. disclose the semiconductor device of claim 4.

Cutter et al. in view of Mayer et al. and further in view of Arghavani et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride.

Arghavani et al. disclose a semiconductor device (Fig. 3K) where silicon oxynitride (365 and 366) (col. 6, lines 15 and 16) is formed by nitridation of silicon oxide (360) (col. 5, lines 66 - col. 6, line 2).

Since both Cutter et al. and Arghavani et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Arghavani et al. with the oxynitride layer grown by nitridation of silicon dioxide disclosed by Arghavani et al., because the combined semiconductor device would prevent dopant outdiffusion from the silicide layer or polysilicon layer when polysilicon is used as a semiconductor layer on and in contact with the antifuse layer.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 6 above, and further in view of Chen (US 2003/0062594). The teachings of Cutter et al. in view of Mayer et al. are discussed above.

Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 6.

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer is less than about 50 angstroms thick.

Chen discloses a semiconductor device (Fig. 11) comprising a dielectric antifuse layer (60) (line 3 of [0027]) where the bottom oxide layer (57) (line 5 of [0027]) in the dielectric antifuse layer (60) is less than about 50 angstroms thick (lines 7-9 of [0027]).

Since both Cutter et al. and Chen teach a semiconductor device comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the thickness of the silicon dioxide disclosed by Chen, because the combined semiconductor device would be programmed at an intended low voltage by causing dielectric breakdown, while controlling leakage between the silicide layer and the conductive layer.

5. Claims 9-11 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 2 above, and further in view of Choi (US 5,242,851). The teachings of Cutter et al. in view of Mayer et al. are discussed above.

In regards to claim 9, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.

Cutter et al. further disclose that the top conductor (614) may comprise polysilicon (col. 8, lines 27-28).

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductor or semiconductor layer on and in contact with the grown dielectric antifuse layer is a lightly doped or intrinsic semiconductor layer.

Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7) and an intrinsic polysilicon layer (16) (col. 6, line 11) deposited on the dielectric antifuse layer (14).

Since both Cutter et al. and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the intrinsic semiconductor layer disclosed by Choi, because the combined semiconductor device would reduce off-state leakage due to the combination of the silicide layer as a bottom electrode and the intrinsic semiconductor layer as a top electrode.

In regards to claim 10, Cutter et al. in view of Mayer et al. and further in view of Choi disclose the semiconductor device of claim 9.

Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the intrinsic semiconductor layer forms a portion of a Schottky diode.

Choi discloses a programmable interconnect device (Fig. 3P) further comprising an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode.

Since both Cutter et al. and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the Schottky diode structure disclosed by Choi, because the combined semiconductor device would form a diode device after programming the antifuse layer.

In regards to claim 11, Cutter et al. in view of Mayer et al. and further in view of Choi disclose the semiconductor device of claim 10.

Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the intrinsic semiconductor layer forms a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer.

It is inherent that the intrinsic semiconductor layer disclosed by Choi to form a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer, because the intrinsic semiconductor layer will be brought in contact with the silicide layer after breakdown of the grown dielectric antifuse layer.

In regards to claim 41, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.

Cutter et al. further disclose that the silicide layer (642) is in contact with the polysilicon layer (640) (col. 8, line 2) (Fig. 6B).

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Cutter et al. further disclose that the bottom conductor (112) (col. 1, line 21) of a semiconductor device (Fig. 1) comprising an antifuse layer (110) (col. 1, line 20) is in contact with n- region (126), forming a Schottky diode.

Since Cutter et al. teach a method of fabricating a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the Schottky diode structure disclosed by Cutter et al. to make a semiconductor device comprising a Schottky diode formed between the silicide layer as a bottom conductor and the semiconductor n-region, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Further regarding claim 41, Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductive layer or semiconductor layer is a portion of a Schottky diode, and therefore the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7), an intrinsic polysilicon layer (16) (col. 6,

lines 11) deposited on the dielectric antifuse layer (14), and an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode.

Since both Cutter et al. and Choi teach a semiconductor memory comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. comprising a Schottky diode between the silicide layer and the bottom semiconductor layer with the Schottky diode formed between the intrinsic semiconductor layer and the top conductor layer disclosed by Choi, because the combined semiconductor device would form a diode device comprising two Schottky diodes in series after programming the antifuse layer.

6. Claim 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Choi (US 5,242,851) as applied to claim 11 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Choi are discussed above.

In regards to claim 12, Cutter et al. in view of Mayer et al. and further in view of Choi disclose the semiconductor device of claim 11.

Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.

Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer.

In regards to claim 13, Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 12.

Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the

combined semiconductor device could be used in a high density semiconductor memory.

In regards to claim 14, Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 13.

Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.

Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 15 above, and further in view of Cleeves et al. (US 6,541,312).

Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 15.

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductive layer forms a portion of a Schottky diode.

Cleeves et al. disclose an antifuse stack structure (Fig. 14F) where a lightly doped semiconductor layer (P-) is deposited on a conductor layer (CONDUCTOR), forming a Schottky diode.

Since both Cutter et al. and Cleeves et al. teach a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the Schottky diode structure disclosed by Cleeves et al., because the combined semiconductor device would form a diode device after programming the dielectric antifuse layer.

8. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Cleeves et al. (US 6,541,312) as applied to claim 16 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. are discussed above.

In regards to claim 18, Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. disclose the semiconductor device of claim 16.

Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.

Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer.

In regards to claim 19, Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 18.

Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art

at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

In regards to claim 20, Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 19.

Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.

Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

9. Claims 27, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 6 above, and further in view of Hart et al. (US 5,726,484).

In regards to claim 27, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 6.

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductive layer comprises titanium nitride.

Hart et al. disclose a semiconductor device comprising an antifuse (Fig. 1A) where titanium nitride layer (101) (col. 5, lines 40-44) is deposited on the antifuse layer (105) (col. 5, line 31).

Since both Cutter et al. and Hart et al. disclose a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the titanium nitride conductive layer disclosed by Hart et al., because the combined semiconductor device could use titanium nitride against diffusion of copper atoms when copper is used as interconnect material.

In regards to claim 33, Cutter et al. in view of Mayer et al. and further in view of Hart et al. disclose the semiconductor device of claim 27.

Cutter et al. in view of Mayer et al. and further in view of Hart et al. differ from the claimed invention by not showing that for a portion of the conductive layer more than

about 20 angstroms thick, the density of the titanium nitride is less than about 4.0 grams per cubic cm.

The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

In regards to claim 34, Cutter et al. in view of Mayer et al. and further in view of Hart et al. disclose the semiconductor device of claim 27.

Cutter et al. in view of Mayer et al. and further in view of Hart et al. differ from the claimed invention by not showing that for a portion of the film more than about 20 angstroms thick, the resistivity of the titanium nitride is greater than about 300 microOhm-cms.

The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art

ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

10. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Hart et al. (US 5,726,484) as applied to claim 27 above, and further in view of Cleeves et al. (US 6,541,312).

Cutter et al. in view of Mayer et al. and further in view of Hart et al. disclose the semiconductor of claim 27.

Cutter et al. in view of Mayer et al. and further in view of Hart et al. differ from the claimed invention by not showing that the conductive layer forms a portion of a Schottky diode.

Cleeves et al. disclose an antifuse stack structure (Fig. 14F) where a lightly doped semiconductor layer (P-) is deposited on a conductor layer (CONDUCTOR), forming a Schottky diode.

Since both Cutter et al. and Cleeves et al. teach a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device

disclosed by Cutter et al. in view of Mayer et al. and further in view of Hart et al. with the Schottky diode structure disclosed by Cleeves et al., because the combined semiconductor device would form a diode device after programming the dielectric antifuse layer.

11. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Hart et al. (US 5,726,484) and then further in view of Cleeves et al. (US 6,541,312) as applied to claim 28 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. are discussed above.

In regards to claim 30, Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. disclose the semiconductor device of claim 28.

Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.

Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art

at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer, a titanium nitride conductive layer and a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer.

In regards to claim 31, Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 30.

Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

In regards to claim 32, Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 31.

Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.

Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

12. Claim 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 36 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. are discussed above.

In regards to claim 37, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 36.

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.

Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer.

In regards to claim 38, Cutter et al. in view of Mayer et al. and further in view of Van Brocklin et al. disclose the semiconductor device of claim 37.

Cutter et al. in view of Mayer et al. and further in view of Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art

at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

In regards to claim 39, Cutter et al. in view of Mayer et al. and further in view of Van Brocklin et al. disclose the semiconductor device of claim 38.

Cutter et al. in view of Mayer et al. and further in view of Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.

Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

13. Claim 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Choi (US

5,242,851) as applied to claim 41 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Choi are discussed above.

In regards to claim 42, Cutter et al. in view of Mayer et al. and further in view of Choi disclose the semiconductor device of claim 41.

Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.

Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the memory cell disclosed by Van Brocklin et al., because the combined semiconductor device would form a diode device comprising a series of Schottky diodes after programming the antifuse layer.

In regards to claim 43, Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 42.

Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

In regards to claim 44, Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 43.

Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.

Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin

et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. Claims 57, 2, 3, 9 and 11-14 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5 of U.S. Patent No. 6,853,049. Although the conflicting claims are not identical, they are not patentably distinct from each other because the semiconductor device of claim 57 of current application may comprise a silicide layer, a grown silicon oxide antifuse layer on and in contact with the silicide layer, and a semiconductor layer on and in contact with

the grown silicon oxide antifuse layer, which is claimed in claim 1 of U.S. Patent No. 6,853,049.

Response to Arguments

16. Applicant's arguments with respect to claims 57, 2-16, 18-20, 27, 28 and 30-44 have been considered but are moot in view of the new grounds of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay C. Kim whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Primary Examiner
6/5/07

J.K.
June 4, 2007